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Design and fabrication of uncooled bolometer based infrared focal plane arrays

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Abstract

Thermal imaging and infrared (IR) thermography are being applied in the fields of surveillance, night vision, fire fighting, predictive maintenance, automation, process control, building services engineering, human and veterinary medicine and many more. During the past ten years, infrared technology has made large progress. Today thermal imaging is mostly based on detector arrays, including high resolution focal plane arrays (FPA). Whereas photonic IR detectors need cooling, thermal IR detectors are also suitable for uncooled operation and thus, adaptive for low cost and hand-held applications.

This work focuses on bolometer based IRFPAs. Bolometers are thermal IR detectors which measure the temperature difference resulting from absorbed IR radiation as a change of the electrical resistance. Surface micromachining is used to fabricate such IRFPAs. In order to enable the use of high performance sensing materials, an adhesive wafer bonding technique is used to integrate the bolometer arrays with a CMOS based read out integrated circuit (ROIC).

After some theoretical considerations, a lithography mask set has been designed. Several variations in detector layout and process flow have been included. The ROIC layout by Linköping Institute of Technology has also been taken into account. During the time of this master thesis project, the process development regarding the fabrication of uncooled bolometer based IRFPAs could be started. The first fabrication steps could be proved.

Acknowledgements

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Looking back on my studies I want to thank Norbert Franz for giving me the chance to make some practical experiences at Martin Christ Freeze Dryers. I thank Prof. Dr. Walter Strampp for the opportunity to work for a long time as his student assistant and learning much about the TEX typesetting system. I would also like to thank Michael Heckert for introducing me to the very useful basics of typography and text design.

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Stockholm, 2003, *Stefan Schüler*

Erklärung zur Diplomarbeit II (official statement)

Diese Arbeit wurde – gemäß § 27 der Prüfungsordnung vom 04.05.1987 in der Fassung vom 16.07.1997 für den Diplomstudiengang Elektrotechnik an der Universität Kassel – dem Vorsitzenden des Prüfungsausschusses zur Annahme und Bewertung als Diplomarbeit II vorgelegt. Die Diplomarbeit wurde angefertigt zum Erlangen des akademischen Grades „Diplom-Ingenieur" der Fachrichtung Elektrotechnik gemäß § 2 sowie des akademischen Grades „Master of Science" gemäß § 29 Abs. 2 der Prüfungsordnung.

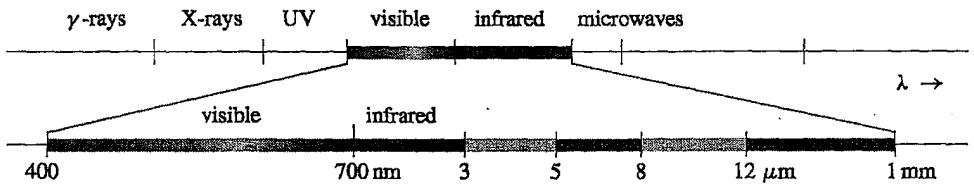
Hiermit erkläre ich gemäß § 14 Abs. 7, dass ich diese Arbeit selbstständig verfasst habe und keine anderen als die angegebenen Quellen und Hilfsmittel verwendet habe.

Härmed förklarar jag att jag har skrivit detta arbete självständigt, och att jag inte använt några andra källor eller hjälpmedel än de här angivna.

Contents

1 Introduction

Infrared (IR) is electromagnetic radiation in the spectral range from 0.7 μm up to 1 mm (fig. 1.1). It was first discovered by Herschel in 1800 by using a prism to disperse sunlight and a blackened mercury thermometer to absorb and measure the radiation. During the second half of the 19th century the radiation laws were found by Planck, Boltzmann, Stefan, Wien and Kirchhoff. [GERTHSEN, 1995]



Spectral diagram **Figure 1.1**

IR transmission windows of the atmosphere are at 3 – 5 μm and 8 – 12 μm.

Planck's law (eq. 1.1) gives the distribution of the radiation as a function of the wavelength in case of a black body which has 100% absorption for all wavelengths. The total exitance M of a black body is the integration of M_λ over all wavelengths (eq. 1.2).

$$M_\lambda = \frac{c_1}{\lambda^5} \frac{1}{e^{c_2/\lambda T} - 1}$$

Planck's law

M_λ: spectral radiant exitance ($Wm^{-2}\mu m^{-1}$),
λ: wavelength (μm), T: temperature (K),
c_1, c_2: first and second radiation constant
$c_1 = 2\pi hc^2 = 3,74 \cdot 10^{-16}$ Wm^2
$c_2 = hc/k = 1,44 \cdot 10^{-2}$ Km

Equation 1.1

$$M = \int_0^\infty M_\lambda \, d\lambda = \sigma T^4$$

Stefan-Boltzmann law

M: total exitance of a black body (Wm^{-2}),
σ: Stefan-Boltzmann constant $5,67 \cdot 10^{-8}$ $Wm^{-2}K^{-4}$

Equation 1.2

Wien's law (eq. 1.3) gives the relation between wavelength and temperature for the emission maximum. The maximum emission for room temperature can be found at 10 μm. That is the reason why the transmission window of the atmosphere between 8 and 12 μm is used most frequently for thermal imaging.

A real body can never absorb 100% at all wavelengths. Even a rough blackened surface is not an ideal black body. Kirchhoff's law (eq. 1.4) gives the relation between an ideal black body and a real body.

$$\lambda_m T = 2898\ \mu\mathrm{m\,K}$$

Wien's displacement law

Equation 1.3

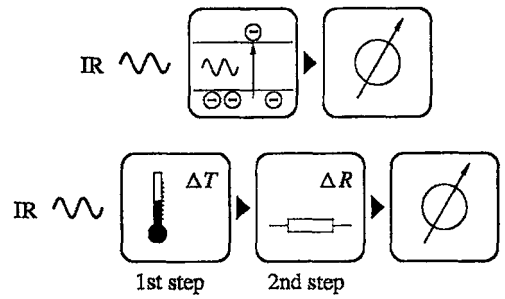
$$M_{\mathrm{real}} = \varepsilon M_{\mathrm{black}}$$

Kirchhoff's law

ε: emissivity or absorptance (0 – 1)

Equation 1.4

The detection of IR radiation can be classified into two general methods, thermal detection and photonic detection (fig. 1.2). Thermal detection works according to a two step process. The radiation is absorbed in the detector whose temperature increases and then, as second step, this change in temperature is measured as a change of some electrical parameters. Photonic detection is a one step process in which absorbed photons excite charge carriers. The major drawback of photonic detection is the cooling that is needed to obtain low noise. Thermal detectors can be operated at room temperature and are therefore more suitable for low cost and hand-held applications.



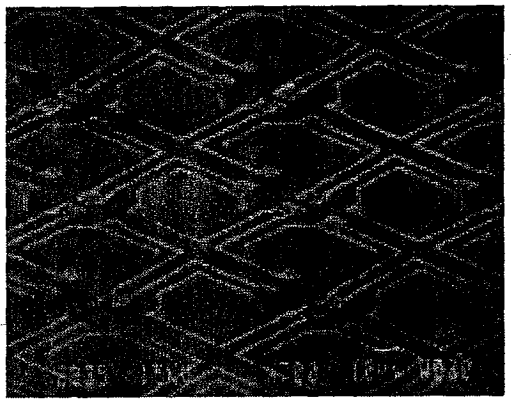
Detection mechanisms for IR radiation

top: photonic detection
bottom: thermal detection with a bolometer, change in electrical resistance is measured

Figure 1.2

The development of thermal infrared detectors started with the thermocouple discovered by Seebeck in 1825. Nobili discovered the thermopile in 1829 and Langley developed the bolometer in 1880 (Greek: bol – ray) [ERIKSSON, 1996]. During the Second World War the Golay cell detector and the pyroelectric detector were developed. [ERIKSSON, 1996] gives an overview of the different thermal detection technologies. This work places emphasis on the bolometer approach which is based on the dependence of electrical resistance and temperature.

In the early 1980s, Kevin Liddiard from the Defence Science and Technology Organisation (DSTO) in Australia had the idea to miniaturise infrared bolometers and integrate them into a focal plane array for thermal imaging applications [LIDDIARD, 1984]. A focal plane array (FPA) is an array of detectors placed at the focal plane of a camera lens system where, in case of IR, a thermal image is formed. Figure 1.3 shows a bolometer based IRFPA.



SEM picture of a bolometer based IRFPA

[ERIKSSON, 1997a]

Figure 1.3

In Sweden, research and development towards infrared focal plane arrays (IRFPA) started in 1992 at the Royal Institute of Technology (Kungl Tekniska Högskolan, KTH) in Stockholm. Pontus Eriksson designed, fabricated and characterised surface micromachined bolometer based IRFPAs, where the bolometer sensing material is amorphous silicon (a-Si). These IRFPAs were intended for monolithic integration on a read out integrated circuit (ROIC) based on CMOS technology. The ROIC was developed at the same time at Linköping Institute of Technology (Linköpings tekniska högskola, LiTH) and the Swedish Defence Research Agency (Totalförsvarets Forskningsinstitut, FOI). In 1999, a first working a-Si IRFPA with 320×240 pixels and a pitch size of $40 \times 40\ \mu m^2$ integrated on a ROIC by LiTH/FOI was demonstrated [JANSSON, 1999].

These first IRFPAs were processed directly on the CMOS wafer. That limits the process temperatures to values below 450°C and, thus, excludes the deposition of high performance materials. In order to allow high temperature processes and even the use of monocrystalline layers for the bolometers, the fabrication of ROIC and bolometers should be done separately. In 1998, the development of a CMOS compatible wafer-level and high yield bonding process started at KTH. That adhesive bonding technique makes it possible to fabricate ROIC and bolometers separately [NIKLAUS, 2002]. The partly processed bolometer devices were bonded to the ROIC and fixed by electro-plating. Unfortunately, the wafer alignment before bonding turned out to be challenging. The requirements for IRFPA fabrication were not met by this device transfer bonding method.

To avoid the difficult wafer alignment step, a film transfer process is needed. The required bolometer layers are deposited at high temperatures and then bonded to the CMOS wafer. The subsequent process steps must be CMOS compatible, but the critical wafer alignment is not longer necessary for this method (fig. 1.4).

The aim of this thesis was to design a CMOS compatible film transfer based process for the fabrication of infrared focal plane arrays. First, some theoretical considerations were made about the choice of materials and pixel design. Based on existing CAD data, a new mask set was designed then. As the last step, the development of a fabrication process was started.

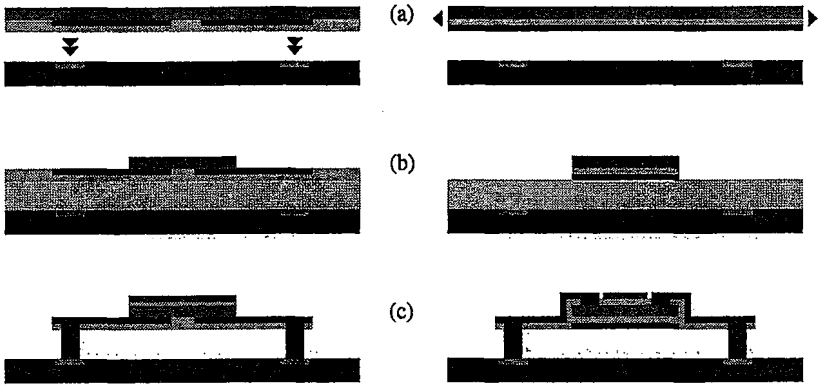


Figure 1.4 Principle of device transfer bonding (left) and film transfer bonding (right)

(a) in device transfer bonding alignment is necessary
(b) electrical contacts underneath the thermistor are not easily possible with film transfer bonding
(c) ready processed bolometer devices

The project was financially supported by FLIR Systems AB in Sweden (http://www.flir.se/). This company builds infrared cameras for thermal imaging and thermography applications.

The following chapter gives an insight into theory and design of uncooled bolometer based infrared focal plane arrays. Chapter 3 describes the process design and chapter 4 the efforts that have been made towards the fabrication of a bolometer array. Finally, in the last chapter the work is summarised and some future prospects are pointed out.

2 Theory and design of bolometers

2.1 Thermal IR detection with bolometers

Bolometers are thermal radiation detectors that measure the temperature change in a so called thermistor (in case of semiconducting material) as a change of the electrical resistance. Figure 2.1 shows the detection schematic with some important parameters that must be taken into account for the detector design. The detection procedure begins with the absorption of IR radiation. The absorptance ε (eq. 1.4) should be as high as possible. The absorbed radiation has the heat content ΔQ. For a good bolometer performance the thermal conductance G should be low, and the thermal mass C should be adapted to G so that the time constant $\tau = C/G$ is suitable for the application.

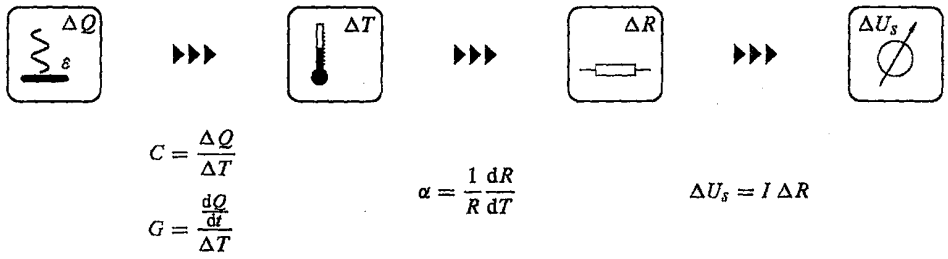


Figure 2.1 Detection schematic of a bolometer with some important parameters

The temperature coefficient of resistivity (TCR, α) gives the coherence between temperature increase and the change in resistance ΔR. Biasing the thermistor by a constant current I, the change in resistance ΔR leads to a voltage change over the thermistor of ΔU_s which can be read out as a measure of the incoming radiation intensity. Biasing by a constant voltage and read out a current as signal is also possible.

The IR bolometer performance in an uncooled focal plane array system is usually measured as the noise equivalent temperature difference (NETD) which is defined as the smallest temperature change that can be detected (eq. 2.1) [ERIKSSON, 1997a]. There are three noise effects that are being taken into account: Thermal conductance noise which is due to heat flow from the detector to its surroundings, Johnson noise which is generated by thermal agitation of the electrons in the thermistor and low-frequency (1/f) noise which exists in any resistor and which increases with decreasing frequency of the biasing voltage. [SEDKY, 1999]

According to [ERIKSSON, 1997a] the NETD can be written as in equation 2.2 and 2.3. The temperature resolution ΔT_s which is defined as the temperature change in the detector that gives a unity signal to noise ratio is given in equation 2.4. The temperature noise ΔT_T is given in equation 2.5.

$$\mathrm{NETD} = \frac{U_n}{\partial U_s / \partial T}$$

Noise equivalent temperature difference (NETD)

U_n: rms value of noise
U_s: signal value

Equation 2.1

$$\mathrm{NETD} = \mathrm{NETD}_T \sqrt{1 + \frac{\Delta T_s^2}{\Delta T_T^2}}$$

NETD_T: ultimate limit of NETD (eq. 2.3)
ΔT_s: temperature resolution
(temperature change that gives unity SNR)
ΔT_T: total temperature noise due to
thermal fluctuations

Equation 2.2

$$\mathrm{NETD}_T = 5,7 \cdot 10^{-12} \frac{T\, f_\#^2}{\varepsilon\, t_{\mathrm{opt}}\, A_{\mathrm{pix}}} \frac{G}{\sqrt{C}}$$

Ultimate limit of NETD
(detector limited by thermal conduction noise)

$f_\#$: f-number of the camera's lens system
t_{opt}: optical transmission of the lens system
A_{pix}: detector area (pixel area in an array)

Equation 2.3

$$\Delta T_s = \frac{\sqrt{\frac{2k_B T R}{t_{\mathrm{int}}} + (kIR)^2 \ln\left(\frac{2,52}{f_l\, t_{\mathrm{int}}}\right)}}{\alpha I R}$$

Temperature resolution
including Johnson noise and 1/f noise

t_{int}: time of integration
f_l: lower limit of the 1/f noise spectrum
k: parameter depending on material and volume

Equation 2.4

$$\Delta T_T = T \sqrt{\frac{k_B}{C}}$$

Temperature noise

Equation 2.5

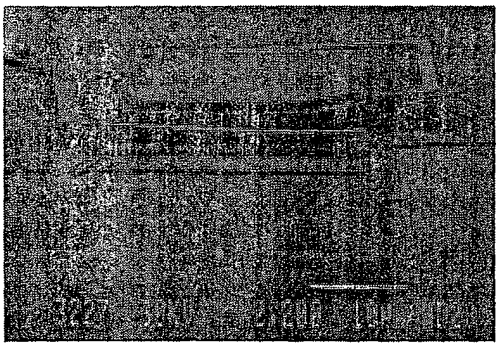
2.2 Bolometer design for IRFPAs

To reach high bolometer performance both NETD and thermal time constant τ must be low. Some parameters in the equations 2.1 – 2.5 can be influenced by layout and material selection in order to raise the signal to noise ratio. Most important are absorptance ε, detector area A_{pix}, TCR α, thermal conductance G and thermal mass C.

High absorptance and a large detector area are required to use as much of the incoming radiation as possible. To reach a high ε an absoption layer on top of the thermistor is used. Interferometric structures in the detector core can increase the effective absorption [ERIKSSON, 1997b].

The TCR is a material parameter. Of course a high α is preferable, but not every material is suitable for bolometer fabrication. Typical materials and their TCRs are a-Si (2%/K) and VOx (2,5%/K). With specially engineered materials like GaAs based quantum well structures or silicon germanium compounds TCRs higher than 4%/K can be expected.

In order to reach a high thermal isolation between the detector and its surroundings, the bolometer core (absorber and thermistor) is usually constructed as micromechanical membrane (fig. 2.2). Mechanical support and electrical connections between thermistor and ROIC are established by thin and long legs with low thermal conductance G_{leg}. The whole bolometer array is enclosed in a vacuum package to prevent losses due to surrounding gas G_{gas}. The total thermal conductance G can be divided into three parts (eq. 2.6). The third component G_{rad} is the ultimate low limit of the thermal conductance and represents the thermal radiation from the membrane itself. The part of the legs is dependent on layout and material selection (eq. 2.7).



SEM picture of a microbolometer

A micromechanical membrane is supported by two long and thin legs.

[ERIKSSON, 1996]

Figure 2.2

$$G = G_{leg} + G_{gas} + G_{rad}$$

Total thermal conductance of a bolometer membrane

Equation 2.6

$$G_{leg} = 2 \cdot \lambda_{leg} \frac{A_{leg}}{l_{leg}}$$

Thermal conductance of two bolometer legs

λ_{leg}: specific thermal conductivity of the legs
A_{leg}, l_{leg}: cross sectional area and length of one leg

λ (W/K m) for some selected materials:

SiN:	3,2	Ti:	22	Pt:	72

References in eq. 2.8.

Equation 2.7

After having decided on detector layout and material selection there is still a certain margin to tailor the thermal mass C in order to reach a thermal time constant $\tau < 10\,\text{ms}$ ($\tau \ll t_{frame}$, $t_{frame} = 20\,\text{ms}$ for a 50 Hz frame rate in a 240 row array). Equation 2.8 shows that C is dependent on the detector volume V. Since the legs' part is usually negligible, the thermistor thickness becomes important.

$$C = V \delta c$$

Thermal mass

V: detector volume, δ: density, c: specific heat

δ (g/cm^3) and c (J/kg K) for some selected materials:

Si:	2,3	700	SiGe:	3,1	600
SiN:	2,2	1200	GaAs:	5,3	330

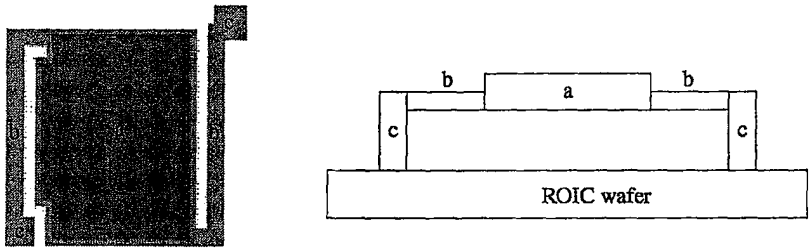
[KITTEL, 1996] [ERIKSSON, 1996] [IOFFE, 2003] [JONES, 2002]

Equation 2.8

The bolometer design for this project was subjected to some other restrictions. The ROIC layout was fixed and the resistance of one detector or one pixel (picture element) had to be approximately 50 kΩ. The pitch size was fixed to $40 \times 40\,\mu\text{m}^2$. Film transfer bonding had to be used and, thus, patterned electrodes underneath the thermistor were excluded (cp. fig. 1.4). Additional noise effects of elecrical contacts should be prevented if possible.

3 Process design

The whole fabrication process is based on adhesive wafer bonding and surface micromachining. The ROIC wafer layout by LiTH (100 mm wafers) and the CMOS compatibility after wafer bonding were taken into account. A lithography mask set with seven masks includes eight different bolometer layouts and some process options for changes in material selection and detector assembly (appendix B). The following sections show a standard process sequence. Figure 3.1 shows a top view and sectional drawing of the standard bolometer layout.



Top view and sectional scheme of a standard bolometer

thermistor core (a)
suspension legs (b)
supporting posts (c)

Figure 3.1

3.1 Wafer preparation and bonding

Before structuring bolometer devices, two base wafers must be prepared and bonded (fig. 3.2). On top of a CMOS based ROIC wafer some metal layers are deposited and patterned in order to get a good contact base for different bolometer outlines. The thermistor material is deposited on a carrier wafer on top of a silicon dioxide etch stop layer (or a SOI wafer is used, where the mono-Si is used as thermistor material). On top of the thermistor layer, silicon nitride is deposited as electrical isolation layer. Metal on top of this isolation layer can be used as reflection layer to build up an interferometric absorption structure (cp. sec. 2.2). The substrate of the carrier wafer (also referred to as sacrificial wafer) is grinded down to a thickness of about 300 μm.

Then, the two wafers are bonded by an adhesive wafer bonding technique [NIKLAUS, 2001b]. Photoresist is spun on top of the ROIC target wafer as bonding adhesive. The sacrificial wafer is brought into close contact with the the target wafer and planted into the bonding machine. During the bonding process, a certain temperature, gas pressure and mechanical pressure are being applied in order to let surface atoms and molecules fuse and adhere to each other.

After wafer bonding, the remaining sacrificial substrate is etched away by plasma etching (typically inductively coupled plasma, ICP). The silicon dioxide etch stop is removed by hydrofluoric acid. The resulting hybrid wafer builds the base for IRFPA fabrication (fig. 3.3a).

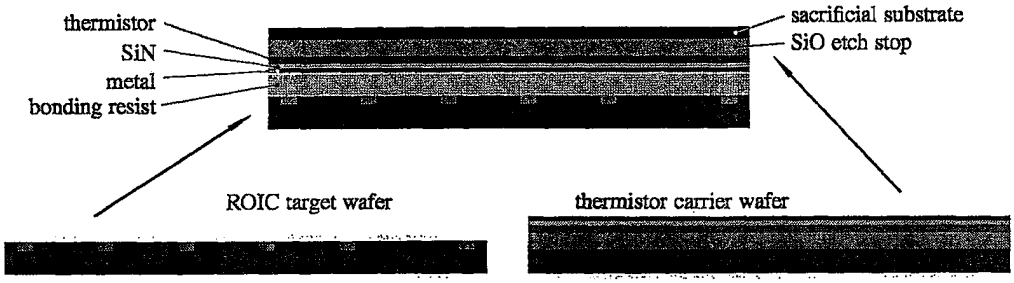
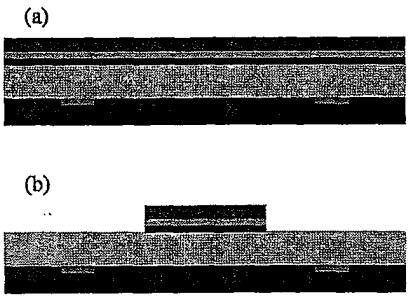


Figure 3.2 The two base wafers after preparation and bonding

The target wafer has contact pads and isolating silicon nitride on its surface. The layers on the carrier wafer are (top to bottom): metal reflector, silicon nitride isolator, thermistor and silicon dioxide etch stop.

3.2 Definition of thermistor core

The first step in structuring the bolometer devices is defining the thermistor core. After having made a standard photo lithography with the THERMISTOR mask, thermistor and silicon nitride are etched by reactive ion etching (RIE). The metal layer is etched wet-chemically after the remaining photoresist is removed. (Fig. 3.3)



Definition of thermistor core

(a) starting point after wafer preparation
(b) defined multi-layer thermistor core

Figure 3.3

3.3 Mechanical suspension and via contacts

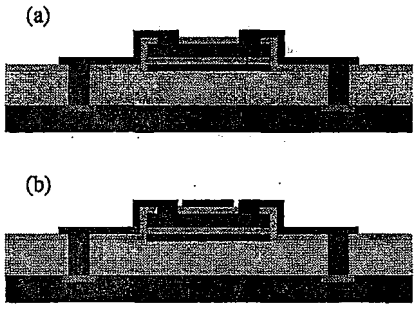
Silicon nitride is used as mechanical suspension for the thermistor. The deposited SiN is structured using the VIA HOLES mask. Both SiN and the underlying bonding resist are etched by RIE. Electro-plating is used to establish via contacts as electrical connection between ROIC and hybrid wafer surface. (Fig. 3.4)

Wafer after SiN deposition and electro-plating

Figure 3.4

3.4 Electrical contacts and IR absorber

In the next step electrical contacts between thermistor and via contacts are build up. The structures are provided on the two masks CONTACT HOLES and CONTACTS. The mask ABSORBER is used to structure the afterward deposited IR absorbing material. (Fig. 3.5)



Metal contacts and IR absorber

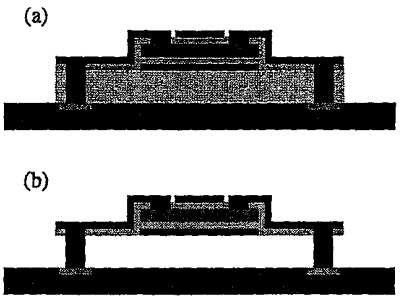
(a) electrical contact between thermistor material and via contacts are established
(b) infrared absorption layer is added

Figure 3.5

3.5 Final bolometer definition

For the final definition of the bolometers' outline another standard photolithography is done with the mask PIXEL MESA. The SiN layer and the bonding resist is etched by RIE. Then the wafer is cleaved into chips. On chip-level the remaining bonding resist is removed by O_2 plasma. The thermistor core is connected to the ROIC by only two suspension legs, consisting of SiN and a very thin metal layer, and the electro-plated posts (fig. 3.6).

Figure 3.7 shows a 3D schematic of a single bolometer after removal of the sacrificial layer. The air-gap and the thin and long suspension legs provide good thermal isolation of the thermistor core and its surrounding.



Final bolometer definition

(a) after mesa etching
(b) after removal of the sacrificial layer

Figure 3.6

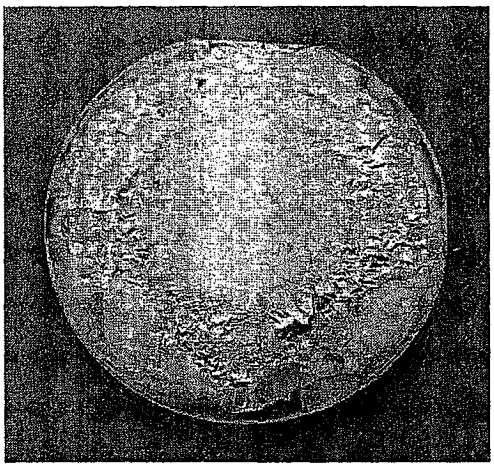
3D schematic of a single bolometer (here without absorber) (cp. fig. 3.1)

Figure 3.7

4 Fabrication of bolometer arrays

In order to try the new designed fabrication process, some test wafers were needed. Instead of expensive CMOS ROIC wafers, plain silicon wafers were used. These wafers were metallised and structured in a way to obtain the same conditions for wafer bonding and electro-plating as with the original ROIC wafers. In the state of process development polycrystalline silicon was used as thermistor material. With the use of this relative cheap material all major aspects of the process can be evaluated. Later on it can be replaced by other materials, such as SiGe or monocrystalline silicon (from SOI wafers).

The next step after the preparation of CMOS dummies and carrier wafers is the wafer bonding process. The know-how for such wafer bonding processes was available [NIKLAUS, 2002], but the process parameters must be fitted to the special conditions. As bonding material the negative photoresist ULTRA-i 300 from Shipley was used. The wafer bonding turned out to be highly dependent on metal selection. The surface condition of the metal layer on the sacrificial wafer are crucial in building up a strong and accurate bond with the bonding resist. Appropriate materials and process parameters for this project could be found and the resulting hybrid wafers were suitable for process development (fig. 4.1 and 4.2).

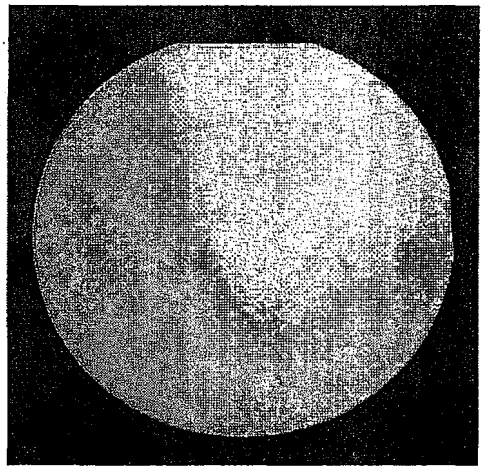


A weak bond or too high stress in the sacrificial wafer leads to voids. In the shown case the transfered layers peeled off during etching of the sacrificial substrate.

Figure from [NIKLAUS, 2001a]

Figure 4.1

A critical step after wafer bonding is the removal of the sacrificial substrate and the silicon dioxide layer. The substrate is typically etched by ICP. During this process step the quality of the bond is put to the test. If the bond is not strong enough or the stress is too high on the sacrificial wafer, the transfered layers might peel off as seen in figure 4.1.

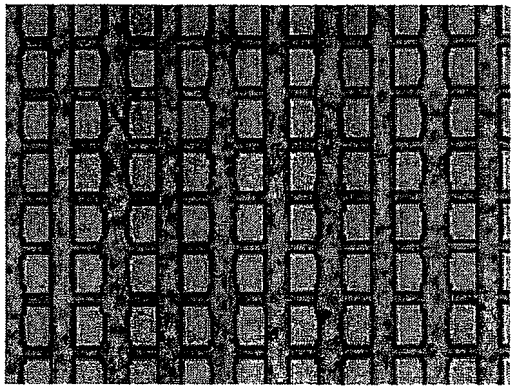


An accurate bond without voids.

Figure from [NIKLAUS, 2001a]

Figure 4.2

When the three wanted layers are successfully transfered to the CMOS dummy, the bolometers can be built up by surface micromachining. The definition of the thermistor core by RIE and wet-chemical etching of the metal layer could be demonstrated as seen in figure 4.3.

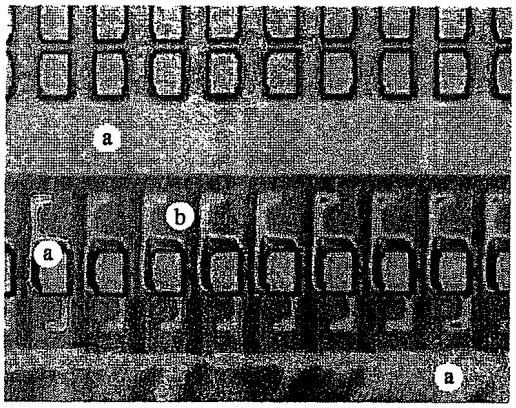


Thermistor cores made from the transferred layers. The bonding resist shows inhomogeneities. (cp. fig. 3.3b)

Figure 4.3

For some process options it is necessary to structure the metal layer with an additional lithography and wet-etching step (PROTECTION mask). The metal can then be used as etching mask for the bonding resist. This procedure is used for building up reference bolometers that are needed for ROIC functionality. A description of the exact properties of the reference bolometers is beyond the scope of this thesis.

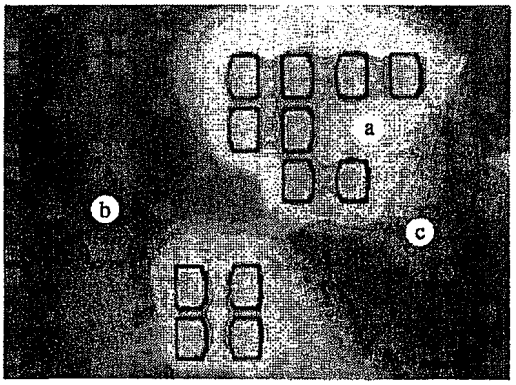
During experiments with structuring the metal layer some problems occured. The needed uniformity over the whole wafer was not longer given. The figures 4.4 and 4.5 document the state of processing at the end of this thesis. The microscope print in figure 4.4 shows thermistor cores on top of a structured metal layer. The metal is slightly overetched and, thus, the openings are bigger than designed. Neither bonding resist nor photoresist on top of the metal are completely removed. Other parts of the wafer show destroyed arrays and completely removed bonding resist (fig. 4.5).



Structured metal layer and openings around the reference bolometers.

(a) metal layer, also S-shaped areas (see dashed line)
(b) openings in the metal, view on the CMOS dummy through remaining bonding resist

Figure 4.4



Destroyed array of thermistor cores.

metal cluster with remaining thermistor cores (a)
bonding resist is removed, CMOS dummy structure (b)
some remaining bonding resist (c)

Figure 4.5

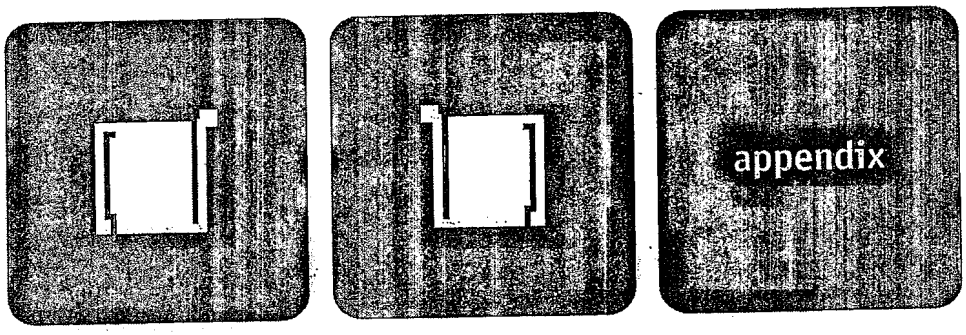
The explanation for the too low uniformity could be mainly given by the wrong thickness of the thermistor layer. The thermistor layer was by mistake much thicker than specified. A too long etching time and several interruptions during the RIE process caused the shown situation.

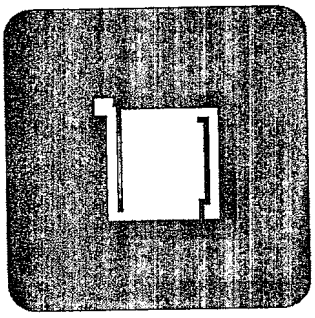
5 Conclusion and future prospects

After some theoretical considerations and decisions concerning the material selection and general build-up of the bolometers, the process design was started. Seven lithography masks were designed with several pixel layouts and some process variations. During the time of this master thesis project, the process development towards the fabrication of uncooled bolometer based IRFPAs could have been started. The first fabrication steps could already be proved.

The project continues directly with further process development. The goal is to have a completed bolometer array by the end of this year (2003). The process development will be carried out on CMOS dummies as long as possible to keep costs low. As soon as the arrays' quality is good enough, the integration with the CMOS ROIC will begin.

Later on, material optimisation and packaging become interesting issues. The designed lithography masks include some concepts for other thermistor materials than the currently used a-Si and even other bolometer assemblies. Also, special materials like colossal magnetoresistive (CMR) metaloxides will be tested. The ultimate ambition is to continue this project and develop commercial infrared focal plane arrays.


appendix



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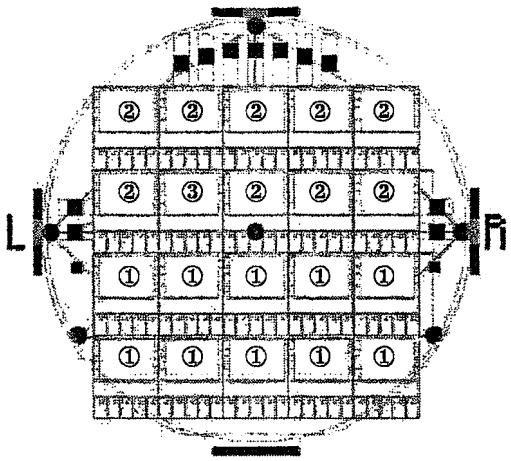
B Mask set "bolometers 2003"

This chapter gives an overview of the mask set "bolometers 2003". The masks were designed with L-Edit V 8.22 and fabricated by Compugraphics International Ltd. in Scotland. The following four sections show the major features of the masks beginning on wafer level and continuing down to the pixel level with its different bolometer versions.

B.1 Wafer level

On wafer level, the masks are structured into a 5 × 4 array of clusters (fig. B.1). There exist three types of clusters that differ in the types of bolometers placed on the chips. In addition to the clusters there are circular and square contacts on the VIA HOLES layer for electro-plating. The border circles are cutted to make sure, that the open area is completely in gold. The open area measures about 1 cm^2 without the squares and the squares altogether measure 1,5 cm^2. The rectangles and the left and right marks are made for an easier alignment especially on dark field masks.



Scheme of the masks on wafer level

5 × 4 array of clusters ①–③

One full and five cutted black circles on VIA HOLES layer as e-plating contacts

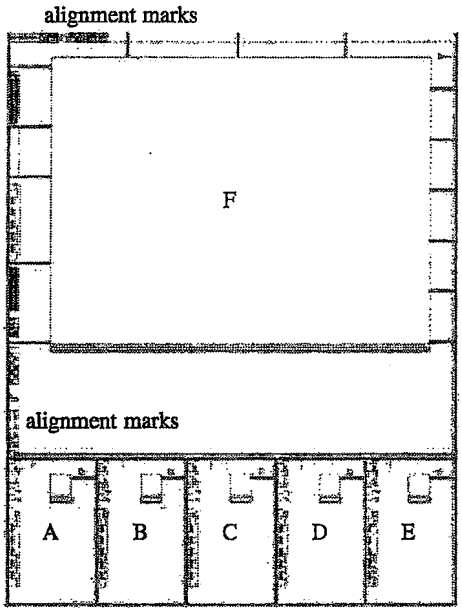
Black squares on VIA HOLES layer as backup for increasing open e-plating area

Rectangular border marks with 'L' and 'R' for better aligning of the masks on the wafer

Figure B.1

B.2 Cluster level

One cluster consists of six chips, five smaller test chips (A–E) and one chip with the large 322 × 242 bolometer array (fig. B.2). At the left and upper edge alignment marks are placed. These marks and the use of them are described in section B.6.



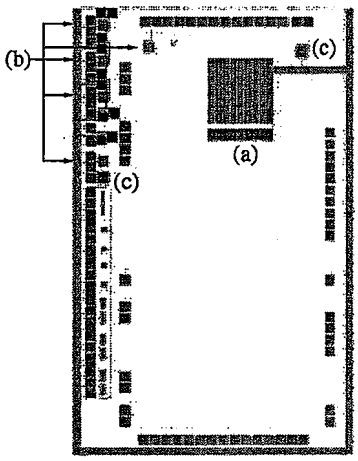
Scheme of a cluster

Chips A–F and two blocks of alignment marks at the left and upper edge of chip F.

Figure B.2

B.3 Chip level

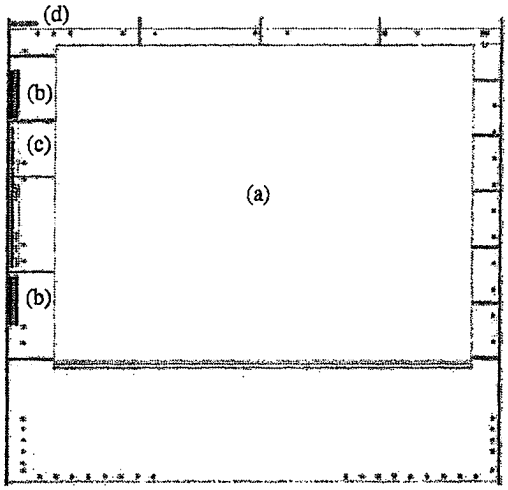
The five smaller chips have one 18 × 18 and five 3 × 3 bolometer arrays each (fig. B.3). The large array and two of the smaller ones are connected to the CMOS where reference bolometers exist. The distribution of bolometer versions on chips and clusters is documented in section B.5. The squares at the chip borders are pads for wire bonding to read out the data from the ROIC.



Scheme of small test chip

18 × 18 array with 18 reference bolometers (a) five 3 × 3 arrays and (b) two blocks of three reference bolometers (c)

Figure B.3



Scheme of chip F

(a) 322 × 242 array with 322 reference bolometers
(b) two blocks of five single test bolometers
(c) four 3 × 3 arrays and two blocks of three ref. bolo.
(d) structures for testing etch-depth and electrical contacts

Figure B.4

On the larger chip F, the 322 × 242 bolometer focal plane array is placed together with 322 reference bolometers. There are also four 3 × 3 arrays (two with ref. bolo.) and ten single test bolometers with large test pads on the chip.

On chip F and also on the smaller chips (next to the 3 × 3 arrays) there are structures for testing etch-depth, electrical contacts and characteristics of the thermistor.

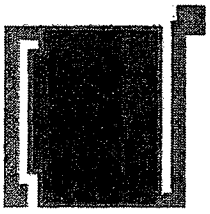
B.4 Pixel level

The bolometers exist in four different configurations: There are single bolometers with large contact pads for testing, 3×3 arrays, 18×18 arrays and large 322×242 arrays (q. v. sec. B.5). In arrays the bolometers are grouped into smaller 2×2 arrays with a common ground.

The eight different bolometer layouts are shown in the following four subsections.

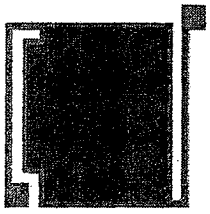
B.4.1 Standard layout

The standard layout is made for bolometers with a thermistor core and metal/nitride suspensions. There are four variations shown in figures B.5 – B.8.



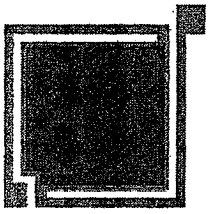
Standard pixel 'std3' with 3 μm wide suspensions

Figure B.5



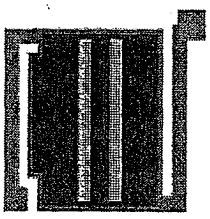
Standard pixel 'std15' with 1.5 μm wide suspensions

Figure B.6



Standard pixel 'stdl' with
2 μm wide and very long suspensions

Figure B.7

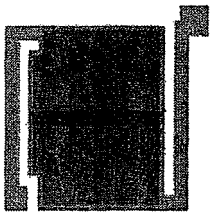


Experimental structure 'xng' with a narrow gap for low doping levels or high resistivities respectively

Figure B.8

B.4.2 Multi layer layout

For the case of multi layer thermistor material an experimental bolometer layout was made (fig. B.9). The layout is practically the same as 'std3'.

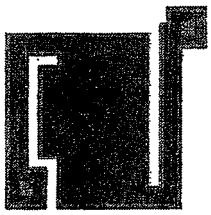


Experimental bolometer layout 'xml' for multi layer thermistor

Figure B.9

B.4.3 Pure thermistor layout

In the pure thermistor bolometer ('pth', fig. B.10) even the suspensions consist of thermistor material.

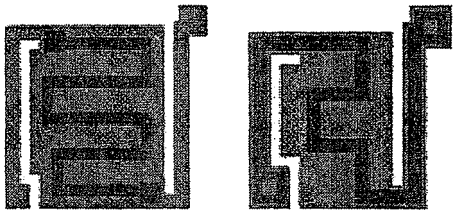


Pixel with 3 μm wide suspensions made of thermistor material

Figure B.10

B.4.4 CMR meander layout

For the tests with colossal magnetoresistive (CMR) metaloxides, two additional bolometer layouts with meander structures as their thermistor exist on one cluster (fig. B.11).



Standard layout with 2 μm wide meander structure as thermistor ('cmr2') (left)

Pure thermistor layout with 3 μm wide meander structure as thermistor ('cmr3') (right)

Figure B.11

B.5 Device distribution

The following tables B.1 – B.6 show the distribution of devices on cluster level. The columns are: number of devices, device type, bolometer layout and place on the cluster.

1	322x242	std3	F
1	18x18	std2	A
1	18x18	stdl	B
1	18x18	std3	C
1	18x18	xng	D
1	18x18	pth	E
5	3x3	std2	A
5	3x3	stdl	B
3	3x3	xml	C
5	3x3	xng	D
5	3x3	pth	E
4+2	3x3	std3	F+C
2	single	std3	F
2	single	std2	F
2	single	stdl	F
2	single	pth	F
1	single	xng	F
1	single	xml	F

Table B.3 Bolometers on cluster 3

1	322x242	std3	F
1	18x18	std2	A
1	18x18	stdl	B
1	18x18	std3	C
1	18x18	xml	D
1	18x18	pth	E
5	3x3	std2	A
5	3x3	stdl	B
3	3x3	xng	C
5	3x3	xml	D
5	3x3	pth	E
4+2	3x3	std3	F+C
2	single	std3	F
2	single	std2	F
2	single	stdl	F
2	single	pth	F
1	single	xng	F
1	single	xml	F

Table B.2 Bolometers on cluster 2

1	322x242	std3	F
1+1+1	18x18	cmr2	A+B+D
1+1	18x18	cmr3	C+E
5+5+5+2	3x3	cmr2	A+B+D+F
5+5+1	3x3	cmr3	C+E+F
1	3x3	std3	F
5	single	cmr2	F
5	single	cmr3	F

Table B.1 Bolometers on cluster 1

1	322x1	std3	F
1	18x1	std2	A
1	18x1	std1	B
1	18x1	std3	C
1	18x1	xng	D
1	18x1	pth	E
2	3x1	std2	A
2	3x1	std1	B
2+2	3x1	std3	C+F
2	3x1	xng	D
2	3x1	pth	E

Table B.4 Reference bolometers on cluster 1

1	322x1	std3 ep	F
1	18x1	std2 ep	A
1	18x1	std1 ep	B
1	18x1	std3 ep	C
1	18x1	xml ep	D
1	18x1	pth ep	E
2	3x1	std2 ep	A
2	3x1	std1 ep	B
2+2	3x1	std3 ep	C+F
2	3x1	xml ep	D
2	3x1	pth ep	E

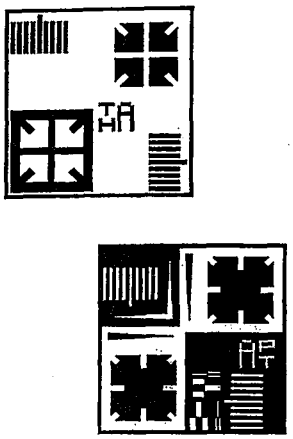
Table B.5 Reference bolometers on cluster 2

1	322x1	std3 ep	F
1+1	18x1	cmr2	A+B
1	18x1	cmr2 ep	D
1	18x1	cmr3	C
1	18x1	cmr3 ep	E
2+2	3x1	cmr2	A+B
2	3x1	cmr2 ep	D
2	3x1	cmr3	C
2	3x1	cmr3 ep	E
2	3x1	std3 ep	F

Table B.6 Reference bolometers on cluster 3

B.6 Alignment marks

There are two blocks of alignment marks on each cluster (sec. B.2, fig. B.2). There exist mainly two types of alignment marks. One type prepares the wafer for the next step, the other type is used for aligning it with an existing mark (fig. B.12).



The two types of alignment marks
Upper type for preparation, lower type for aligning
(lower one is shown inverse here).

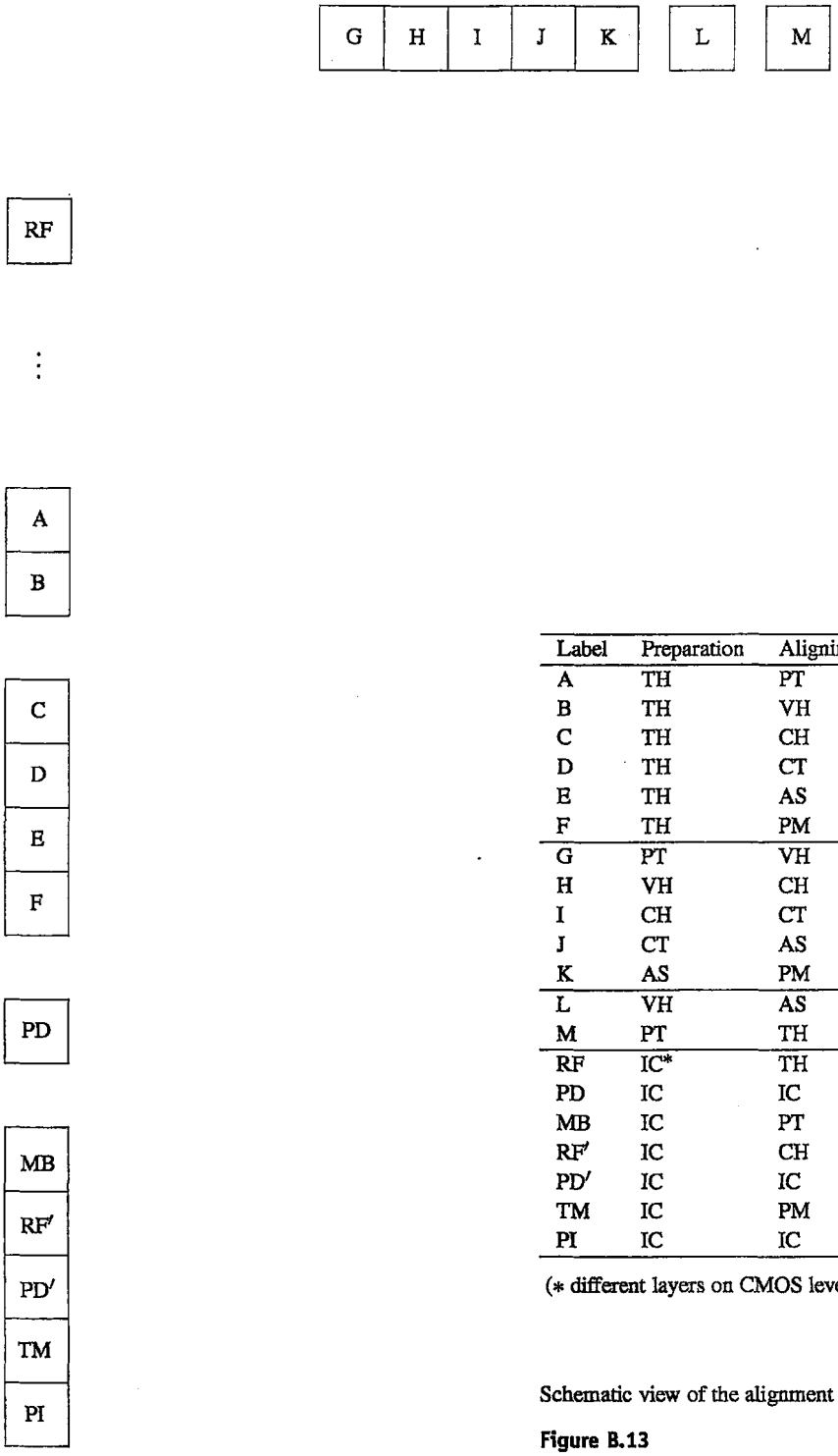
Layer abbreviations:

TH	THERMISTOR
PT	PROTECTION
VH	VIA HOLES
CH	CONTACT HOLES
CT	CONTACTS
AS	ABSORBER
PM	PIXEL MESA

Figure B.12

The alignment marks on the seven new mask layers are labelled with capital letters A – M, and an abbreviation of the layer they are on. The marks on CMOS level are labelled with RF, PD, MB, TM and PI. To prevent mistakes the CMOS labels are also used on the new layers where these are aligned with the CMOS.

Figure B.13 shows the positions of alignment marks on a cluster (cp. fig. B.2)



Label	Preparation	Aligning
A	TH	PT
B	TH	VH
C	TH	CH
D	TH	CT
E	TH	AS
F	TH	PM
G	PT	VH
H	VH	CH
I	CH	CT
J	CT	AS
K	AS	PM
L	VH	AS
M	PT	TH
RF	IC*	TH
PD	IC	IC
MB	IC	PT
RF'	IC	CH
PD'	IC	IC
TM	IC	PM
PI	IC	IC

(* different layers on CMOS level)

Schematic view of the alignment marks' positions.

Figure B.13